Sampling Circuit on Silicon Substrate for Frequencies beyond 50 GHz

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***Abstract* — We have fabricated and measured a sampling circuit on high resistivity silicon substrate. The circuit incorporates a nonlinear transmission line to provide the sampling pulses. The sampling circuit was measured up to 50 GHz, with a voltage conversion loss lower than 11 dB and varying in this range by just 2.3 dB. This is the first presentation of a sampling circuit on silicon substrate with a corner frequency beyond 50 GHz.**

I. Introduction

Time-domain characterization using equivalent-time sampling techniques are an important tool for the characterization of semiconductor devices and circuits with multi-GHz bandwidths. In contrast to S-parameter measurement setups nonlinearities of the circuit under test can be observed. To achieve a high temporal resolution, both high-speed switching circuits and narrow sampling pulses are needed. One successful way to generate picosecond sampling pulses is the use of nonlinear transmission lines for pulse compression.

Most of the published results in this area use GaAs as a substrate. GaAs has two basic advantages compared to silicon. One is the eight times higher mobility of the electron for the same doping concentration and the other is that the substrate is semi-insulating. This results in higher corner frequencies for the diodes and low losses in the rf-lines. The best results reported in literature have fall times of the generated transients of 2.6 ps, 0.68 ps, and 480 fs [1, 2, 3].

To be able to use these low fall times it is important to keep the distance between the device under test and the signal generation circuit as short as possible to reduce attenuation and dispersion. GaAs is a brittle material so additional flexure probes have to be used [4] with connections reducing the bandwidth. Because of the advantageous mechanical properties of silicon, making it the dominating material for micromachining, it is possible to realize the sampling circuit directly on the probe.

Another aspect is costs. For the generation of short fall times long nonlinear transmission lines (NLTL) are needed pushing up the price. One possibility is to replace the commonly used coplanar technology by a microstrip technology and arrange the microstrip lines in a meander shape [5]. A more efficient solution to reduce the cost is the use of silicon as the substrate.

The successful implementation of picosecond shock-wave generation in NLTL in silicon has been reported in [6].

II. Theory

The foundation for fast sampling circuits is the generation of fast fall time electrical transitions which can subsequently be shaped into sampling

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pulses. This can be accomplished by an NLTL. In our design an NLTL consists of a high impedance coplanar wave guide shunted with Schottky diodes serving as voltage dependent capacitors. The sampling circuit including the NLTL is depicted in Fig. 1 [7].

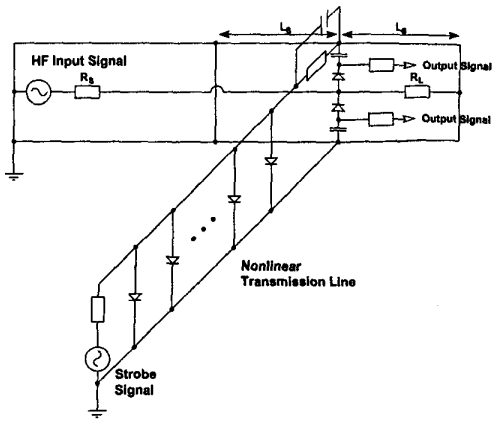

Fig. 1: Schematic of the sampling circuit.

This transmission line shows a voltage dependent phase velocity according to:

$$v_{Phase}(V) = \frac{1}{\sqrt{L' \cdot (C' + C_{Schottky}(V)/d)}}. \quad (1)$$

L' and C' are the inductance and capacitance per unit length, respectively. d is the distance of the Schottky diode to the adjacent diodes and $C_{Schottky}(V)$ the voltage dependent capacitance of the Schottky diode. Due to this relation the fall time of an applied signal can be steepened, as different points on a voltage wave travel with different speed.

The sampling bridge consists of two Schottky diodes and capacitors (the capacitors are also realized as reverse biased Schottky diodes) in a slot line of the length $2 \cdot L_s = 2 \cdot 900\,\mu m$. The slot line is terminated by two shorts.

The two conductors forming the slot line also act as the ground lines of a coplanar waveguide which receives the high-frequency input signal. The center conductor of this waveguide is terminated by R_L (corresponding to its characteristic impedance).

The reflections from the two short-circuits terminating the slot line convert the originally saw-tooth shaped output of the NLTL into a trapezoidal-shaped sampling pulses with fast rise and fall times. Due to the built-in potential of the Schottky diodes and the duration of the fall and rise time the opening of the diode is much shorter than the delay-time caused by the short-circuited slot line.

III. Technology

For the realization of the sampling circuit a Schottky diode process on silicon substrate was developed.

In a first step a buried contact layer with $12.5\Omega/\square$ is implanted into a high resistivity silicon substrate. It is used for both resistors and contacts to the diodes. A 550nm thick layer of $3 \cdot 10^{16}/cm^3$ Sb doped silicon grown by MBE and dry chemically structured forms the mesa structure of the Schottky diodes. After depositing an oxide for passivation and annealing the Schottky and Ohmic contacts are defined by evaporating Pt/Au in a liftoff process. $3\,\mu m$ polyimide is spun on the wafer and cured. Windows to the Pt/Au metalization are dry chemically etched. Finally $4\,\mu m$ Al with 100nm W/Ti for better adhesion is sputtered on the polyimide and wet chemically etched. A cross section of a Schottky diode with coplanar lines is shown in Fig. 2.

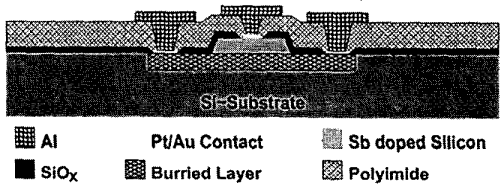

Fig. 2: Cross section of a Schottky diode connected to a coplanar waveguide.

The Schottky diodes have a cutoff frequency of 350 GHz and a breakdown voltage of 13V. The coplanar lines are realized on $3\,\mu m$ polyimide to get a better isolation from the substrate. This results in both a lower attenuation and a higher characteristic impedance of the unloaded lines compared to lines realized directly on silicon.

IV. Layout

The layout of the sampling circuit with NLTL, slot line, and sampling diodes is depicted in Fig. 3.

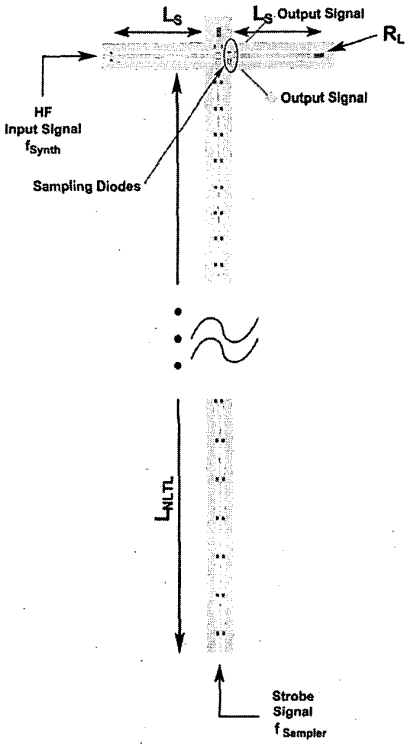

Fig. 3: Layout of the sampling circuit.

The NLTL is not shown in its complete extension because it has a length of L_{NLTL}=16.5 mm. The slot line has an extension in both directions of $L_S = 900\,\mu$m.

V. Measurement Results

For the measurement setup two synthesizers, one oscilloscope, and the sampling circuit is used, see Fig. 4.

Synthesizer I is used with an additional 30 dB amplifier to drive the NLTL with P=25 dBm at the frequency $f_{Sampler}$=4 GHz. The signal of synthesizer II is the sampled signal and has a frequency of

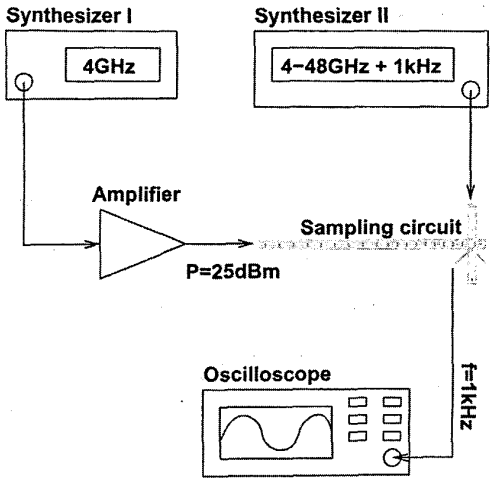

Fig. 4: Layout of the sampling circuit.

$$f_{Synth} = n \cdot f_{Sampler} \pm \Delta f. \qquad (2)$$

This results in an output frequency of Δf at the sampling diodes. The signal is displayed on an oscilloscope. Both RF signals are fed to the sampling circuit by GSG probes with a pitch of 100 μm. The pads to the sampling diodes are contacted by needle probes.

The signal of synthesizer II is swept according to equation (2) between 4 GHz and 48 GHz, so that a frequency of Δf=1 kHz can be measured at the oscilloscope. Because of the frequency dependent attenuation of the measurement setup the power was measured directly at the probes with a calorimeter and used for corrections. The voltage conversion loss between the input signal of synthesizer II and the output signal at the oscilloscope is shown in Fig. 5.

The voltage conversion loss varies between 8.7 dB at 28 GHz and 11 dB at 48 GHz. This results in a variation of just 2.3 dB in the measured frequency range. The corner frequency of this circuit is beyond 50 GHz.

The linearity of the sampling circuit was also measured at 48 GHz. The result is shown in Fig. 6.

The maximum output power of synthesizer II is -4 dBm at 48 GHz. Up to this level the sampling

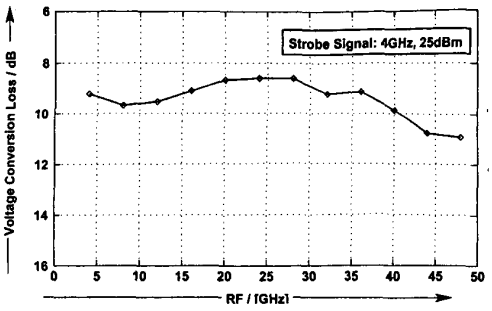

Fig. 5: Voltage conversion loss for an input signal at the nonlinear transmission line with f=4 GHz and P=25 dBm. The sampled signal has a frequency up to 48 GHz.

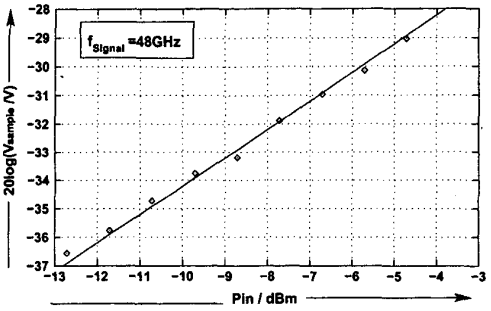

Fig. 6: Linearity of the sampling circuit up to -4 dBm, this is the limit of the synthesizer. V_{Sample} is the effective voltage measured at the oscilloscope.

circuit is not driven into compression. Therefore compression was determined with an 8 GHz signal at a power level of 3 dBm. This corresponds to a peak to peak voltage of 890 mV.

VI. Conclusion

Silicon as a substrate is used for a sampling circuit as an alternative to the commonly used GaAs substrate with the potential of better mechanical properties with regard to micromachined sampling probes and lower substrate costs. The sampling circuit was measured up to 50 GHz without reaching the corner frequency. The voltage conversion loss is better than 11 dB and varies in this frequency range by only 2.3 dB. The sampling circuit is linear up to an input signal of 3 dBm.

VII. Acknowledgment

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VIII. References

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